AMENDMENTS

To the Specification:

Please amend paragraph [0046] as follows:

[0046]　　At the data writing timing, the operational voltage V_{DD} is in a low state for turning off the light emitting diode 350, that is, no current is passed through the terminals of the operational voltage V_{DD} and the ground V_{SS}. The data voltage Vdata from the signal line 310b is electrically connected to the ~~source~~drain terminal of the switching transistor 310. The voltage drop on the capacitor 340 is Vdata-(Vo-V_T +ΔVdata), where ΔVdata=K(Vdata-Vo) and K=Cs/Ctotal, Cs represents the capacitance of the capacitor 340, and Ctotal represents a sum of capacitances on the source terminal of the driving transistor 320. Moreover, in an alternative embodiment of the present invention, another capacitor 360 can be disposed between the source and drain terminals of the reset transistor 330 for changing the Ctotal and adjusting the K in response with the design requirement.

Please amend paragraph [0052] as follows:

[0052]　　At the data writing timing, the V_{AZ} on the AZ line is lowered to a low voltage for turning off the reset transistor 430 and avoiding any current flowing through the terminals of the V_{DD} and the V_{SS}. A data voltage Vdata is applied to the signal line 410b, which is electrically connected to the ~~source~~drain terminal of the switching transistor 410. The voltage drop on the

2

capacitor 440 is $Vdata-(Vo-V_T + \Delta Vdata)$, wherein $\Delta Vdata = K(Vdata-Vo)$ and $K=Cs/Ctotal$, Cs represents the capacitance of the capacitor 440, and Ctotal represents a sum of capacitances on the source terminal of the driving transistor 420. Moreover, in an alternative embodiment, another capacitor 460 can be disposed between the anode and cathode of the light emitting diode 450 for changing the Ctotal and adjusting the K in response with the design requirement.

3